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10/781,338	02/17/2004	Roger Thorpe	ISTOR.013A	9429

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EXAMINER	
PATEL, HARESH N	

ART UNIT	PAPER NUMBER
2454	

NOTIFICATION DATE	DELIVERY MODE
10/16/2008	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

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Office Action Summary	Application No.	Applicant(s)	
	10/781,338	THORPE ET AL.	
	Examiner	Art Unit	
	HARESH N. PATEL	2454	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *30 June 2008*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *21-37* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *21-35* is/are rejected.

7)☒ Claim(s) *36 and 37* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *19 July 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 21-37 are subject to examination. Claims 36 and 37 are allowable but objected to.

Drawings

2. The figures submitted on 7/19/2004 are acknowledged.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 21-35 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ghosh et al. 2003/0233494 (Hereinafter Ghosh) in view of "Official Notice".

5. Referring to claim 21, Ghosh discloses a system for accelerated TCP and iSCSI protocol processing in hardware, the system comprising: a storage network processor (SNP) configured to offload at least some packet processing tasks from a general purpose processor associated with a host device (e.g., page 2), the storage network processor further comprising: a hardware-accelerated receive module configured to receive TCP network packets (e.g., page 2); a hardware-accelerated TCP and iSCSI protocol processing chip configured to process both TCP

network packets and iSCSI instructions and offloading common case iSCSI instructions and TCP network packets to process and resolve embedded iSCSI instructions in the hardware (e.g., page 3); and a hardware-accelerated transmit module configured to transmit TCP network packets (e.g., page 3).

However Ghosh does not specifically show the use of "both TCP network packets and iSCSI instructions embedded in TCP network packets". "Official Notice" is taken that both the concept and advantages of providing the "both TCP network packets and iSCSI instructions embedded in TCP network packets" is well known and expected in the art and would be an obvious design choice to have both TCP network packets and iSCSI instructions embedded in TCP network packets.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to include both TCP network packets and iSCSI instructions embedded in TCP network packets with the teachings of Ghosh in order to facilitate usage of both TCP network packets and iSCSI instructions embedded in TCP network packets because having both TCP network packets and iSCSI instructions embedded in TCP network packets would enhance communicating iSCSI instructions using the TCP network packets. The embedded instructions would support accelerated TCP and iSCSI protocol processing in the hardware.

6. Referring to claim 22, Ghosh discloses the claimed limitations as disclosed above. Ghosh also discloses wherein, offloading of the packet processing tasks occurs at several layers associated with a TCP protocol stack including an IP layer and a TCP layer (e.g., page 2).

7. Referring to claim 23, Ghosh discloses the claimed limitations as disclosed above. Ghosh also discloses wherein, offloading of the packet processing tasks occurs at an iSCSI layer associated with an iSCSI protocol stack (e.g., page 2).

8. Referring to claim 24, Ghosh discloses the claimed limitations as disclosed above. Ghosh also discloses wherein, the packet processing tasks comprise packet parsing operations (e.g., page 3).

9. Referring to claim 25, Ghosh discloses the claimed limitations as disclosed above. Ghosh also discloses wherein, ,the packet parsing operations are directed towards resolving and processing the embedded iSCSI instructions (e.g., page 3).

10. Referring to claim 26, Ghosh discloses the claimed limitations as disclosed above. Ghosh also discloses wherein, the storage network processor accelerates packet parsing operation to accommodate near line-rate receiving and transmission of TCP network packets (e.g., page 2).

11. Referring to claim 27, Ghosh discloses the claimed limitations as rejected above. However Ghosh does not specifically mention about the line rate is approximately 10 Gigabit/sec. "Official Notice" is taken that both the concept and advantages of providing the line rate is approximately 10 Gigabit/sec is well known and expected in the art.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to include the line rate is approximately 10 Gigabit/sec with the teachings of Ghosh in

order to facilitate usage of the line rate is approximately 10 Gigabit/sec because it would support storage operations at higher rate though the offloading.

12. Referring to claim 28, Ghosh discloses the claimed limitations as disclosed above. Ghosh also discloses wherein, the storage network processor is configured to offload protocol processing associated with acknowledgement generation (e.g., page 3).

13. Referring to claim 29, Ghosh discloses the claimed limitations as disclosed above. Ghosh also discloses wherein, the storage network processor is configured to offload protocol processing associated with window management (e.g., page 2).

14. Referring to claim 30, Ghosh discloses the claimed limitations as disclosed above. Ghosh also discloses wherein, the storage network processor is configured to offload protocol processing associated with timer maintenance (e.g., page 3).

15. Referring to claim 31, Ghosh discloses the claimed limitations as disclosed above. Ghosh also discloses wherein, the storage network processor is configured to accelerate protocol processing associated with acknowledgement generation (e.g., page 2).

16. Referring to claim 32, Ghosh discloses the claimed limitations as disclosed above. Ghosh also discloses wherein, the storage network processor is configured to accelerate protocol processing associated with window management (e.g., page 3).

17. Referring to claim 33, Ghosh discloses the claimed limitations as disclosed above. Ghosh also discloses wherein, the storage network processor is configured to accelerate protocol processing associated with timer maintenance (e.g., page 3).

18. Referring to claim 34, Ghosh discloses the claimed limitations as disclosed above. Ghosh also discloses wherein, the storage network processor is configured to accelerate protocol processing associated with window management (e.g., page 3).

19. Referring to claim 35, Ghosh discloses the claimed limitations as disclosed above. Ghosh also discloses wherein, the storage network processor is configured to accelerate protocol processing associated with retransmission (e.g., page 8).

20. Referring to claim 36, Ghosh discloses the claimed limitations as disclosed above. Ghosh also discloses a remote memory channel used to transfer data and meta-data to a partner storage controller to provide at least a degree of fault tolerance (e.g., page 3).

21. Referring to claim 37, Ghosh discloses the claimed limitations as disclosed above. Ghosh also discloses wherein storage data may be re-created on the partner storage controller (e.g., page 3).

22. Claim 21-35 is rejected under 35 U.S.C. 103(a) as being unpatentable over Rangan et al. 2004/0148376 (Hereinafter Rangan) in view of "Official Notice".

23. Referring to claim 21, Rangan discloses a system for accelerated TCP and iSCSI protocol processing in hardware, the system comprising: a storage network processor (SNP) configured to offload at least some packet processing tasks from a general purpose processor associated with a host device (e.g., page 2), the storage network processor further comprising: a hardware-accelerated receive module configured to receive TCP network packets (e.g., page 2); a hardware-accelerated TCP and iSCSI protocol processing chip configured to process both TCP network packets and iSCSI instructions and offloading common case iSCSI instructions and TCP network packets to process and resolve embedded iSCSI instructions in the hardware (e.g., page 3); and a hardware-accelerated transmit module configured to transmit TCP network packets (e.g., page 3).

However Rangan does not specifically show the use of "both TCP network packets and iSCSI instructions embedded in TCP network packets". "Official Notice" is taken that both the concept and advantages of providing the "both TCP network packets and iSCSI instructions embedded in TCP network packets" is well known and expected in the art and would be an obvious design choice to have both TCP network packets and iSCSI instructions embedded in TCP network packets.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to include both TCP network packets and iSCSI instructions embedded in TCP network packets with the teachings of Rangan in order to facilitate usage of both TCP network

packets and iSCSI instructions embedded in TCP network packets because having both TCP network packets and iSCSI instructions embedded in TCP network packets would enhance communicating iSCSI instructions using the TCP network packets. The embedded instructions would support accelerated TCP and iSCSI protocol processing in the hardware.

24. Referring to claim 22, Rangan discloses the claimed limitations as disclosed above. Rangan also discloses wherein, offloading of the packet processing tasks occurs at several layers associated with a TCP protocol stack including an IP layer and a TCP layer (e.g., page 4).

25. Referring to claim 23, Rangan discloses the claimed limitations as disclosed above. Rangan also discloses wherein, offloading of the packet processing tasks occurs at an iSCSI layer associated with an iSCSI protocol stack (e.g., page 4).

26. Referring to claim 24, Rangan discloses the claimed limitations as disclosed above. Rangan also discloses wherein, the packet processing tasks comprise packet parsing operations (e.g., page 6).

27. Referring to claim 25, Rangan discloses the claimed limitations as disclosed above. Rangan also discloses wherein, ,the packet parsing operations are directed towards resolving and processing the embedded iSCSI instructions (e.g., page 3).

28. Referring to claim 26, Rangan discloses the claimed limitations as disclosed above. Rangan also discloses wherein, the storage network processor accelerates packet parsing operation to accommodate near line-rate receiving and transmission of TCP network packets (e.g., page 6).

29. Referring to claim 27, Rangan discloses the claimed limitations as rejected above. However Rangan does not specifically mention about the line rate is approximately 10 Gigabit/sec. "Official Notice" is taken that both the concept and advantages of providing the line rate is approximately 10 Gigabit/sec is well known and expected in the art.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to include the line rate is approximately 10 Gigabit/sec with the teachings of Rangan in order to facilitate usage of the line rate is approximately 10 Gigabit/sec because it would support storage operations at higher rate though the offloading.

30. Referring to claim 28, Rangan discloses the claimed limitations as disclosed above. Rangan also discloses wherein, the storage network processor is configured to offload protocol processing associated with acknowledgement generation (e.g., page 5).

31. Referring to claim 29, Rangan discloses the claimed limitations as disclosed above. Rangan also discloses wherein, the storage network processor is configured to offload protocol processing associated with window management (e.g., page 2).

32. Referring to claim 30, Rangan discloses the claimed limitations as disclosed above. Rangan also discloses wherein, the storage network processor is configured to offload protocol processing associated with timer maintenance (e.g., page 3).

33. Referring to claim 31, Rangan discloses the claimed limitations as disclosed above. Rangan also discloses wherein, the storage network processor is configured to accelerate protocol processing associated with acknowledgement generation (e.g., page 4).

34. Referring to claim 32, Rangan discloses the claimed limitations as disclosed above. Rangan also discloses wherein, the storage network processor is configured to accelerate protocol processing associated with window management (e.g., page 5).

35. Referring to claim 33, Rangan discloses the claimed limitations as disclosed above. Rangan also discloses wherein, the storage network processor is configured to accelerate protocol processing associated with timer maintenance (e.g., page 4).

36. Referring to claim 34, Rangan discloses the claimed limitations as disclosed above. Rangan also discloses wherein, the storage network processor is configured to accelerate protocol processing associated with window management (e.g., page 8).

37. Referring to claim 35, Rangan discloses the claimed limitations as disclosed above. Rangan also discloses wherein, the storage network processor is configured to accelerate protocol processing associated with retransmission (e.g., page 6).

38. Claim 21-35 is rejected under 35 U.S.C. 103(a) as being unpatentable over Pandya 2004/0148376 (Hereinafter Pandya) in view of "Official Notice".

39. Referring to claim 21, Pandya discloses a system for accelerated TCP and iSCSI protocol processing in hardware, the system comprising: a storage network processor (SNP) configured to offload at least some packet processing tasks from a general purpose processor associated with a host device (e.g., page 2), the storage network processor further comprising: a hardware-accelerated receive module configured to receive TCP network packets (e.g., page 2); a hardware-accelerated TCP and iSCSI protocol processing chip configured to process both TCP network packets and iSCSI instructions and offloading common case iSCSI instructions and TCP network packets to process and resolve embedded iSCSI instructions in the hardware (e.g., page 4); and a hardware-accelerated transmit module configured to transmit TCP network packets (e.g., page 4).

However Pandya does not specifically show the use of "both TCP network packets and iSCSI instructions embedded in TCP network packets". "Official Notice" is taken that both the concept and advantages of providing the "both TCP network packets and iSCSI instructions embedded in TCP network packets" is well known and expected in the art and would be an

obvious design choice to have both TCP network packets and iSCSI instructions embedded in TCP network packets.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to include both TCP network packets and iSCSI instructions embedded in TCP network packets with the teachings of Pandya in order to facilitate usage of both TCP network packets and iSCSI instructions embedded in TCP network packets because having both TCP network packets and iSCSI instructions embedded in TCP network packets would enhance communicating iSCSI instructions using the TCP network packets. The embedded instructions would support accelerated TCP and iSCSI protocol processing in the hardware.

40. Referring to claim 22, Pandya discloses the claimed limitations as disclosed above. Pandya also discloses wherein, offloading of the packet processing tasks occurs at several layers associated with a TCP protocol stack including an IP layer and a TCP layer (e.g., page 5).

41. Referring to claim 23, Pandya discloses the claimed limitations as disclosed above. Pandya also discloses wherein, offloading of the packet processing tasks occurs at an iSCSI layer associated with an iSCSI protocol stack (e.g., page 5).

42. Referring to claim 24, Pandya discloses the claimed limitations as disclosed above. Pandya also discloses wherein, the packet processing tasks comprise packet parsing operations (e.g., page 6).

43. Referring to claim 25, Pandya discloses the claimed limitations as disclosed above. Pandya also discloses wherein, ,the packet parsing operations are directed towards resolving and processing the embedded iSCSI instructions (e.g., page 4).

44. Referring to claim 26, Pandya discloses the claimed limitations as disclosed above. Pandya also discloses wherein, the storage network processor accelerates packet parsing operation to accommodate near line-rate receiving and transmission of TCP network packets (e.g., page 6).

45. Referring to claim 27, Pandya discloses the claimed limitations as rejected above. However Pandya does not specifically mention about the line rate is approximately 10 Gigabit/sec. "Official Notice" is taken that both the concept and advantages of providing the line rate is approximately 10 Gigabit/sec is well known and expected in the art.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to include the line rate is approximately 10 Gigabit/sec with the teachings of Pandya in order to facilitate usage of the line rate is approximately 10 Gigabit/sec because it would support storage operations at higher rate though the offloading.

46. Referring to claim 28, Pandya discloses the claimed limitations as disclosed above. Pandya also discloses wherein, the storage network processor is configured to offload protocol processing associated with acknowledgement generation (e.g., page 5).

47. Referring to claim 29, Pandya discloses the claimed limitations as disclosed above. Pandya also discloses wherein, the storage network processor is configured to offload protocol processing associated with window management (e.g., page 2).

48. Referring to claim 30, Pandya discloses the claimed limitations as disclosed above. Pandya also discloses wherein, the storage network processor is configured to offload protocol processing associated with timer maintenance (e.g., page 4).

49. Referring to claim 31, Pandya discloses the claimed limitations as disclosed above. Pandya also discloses wherein, the storage network processor is configured to accelerate protocol processing associated with acknowledgement generation (e.g., page 5).

50. Referring to claim 32, Pandya discloses the claimed limitations as disclosed above. Pandya also discloses wherein, the storage network processor is configured to accelerate protocol processing associated with window management (e.g., page 5).

51. Referring to claim 33, Pandya discloses the claimed limitations as disclosed above. Pandya also discloses wherein, the storage network processor is configured to accelerate protocol processing associated with timer maintenance (e.g., page 5).

52. Referring to claim 34, Pandya discloses the claimed limitations as disclosed above. Pandya also discloses wherein, the storage network processor is configured to accelerate protocol processing associated with window management (e.g., page 9).

53. Referring to claim 35, Pandya discloses the claimed limitations as disclosed above. Pandya also discloses wherein, the storage network processor is configured to accelerate protocol processing associated with retransmission (e.g., page 6).

Allowable Subject Matter

54. Claims 36 and 37 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Response to Arguments

55. Applicant's arguments filed 6/30/2008, pages 4-7, have been fully considered but they are not persuasive. Therefore, rejection of the claims is maintained.

56. Regarding the claim 27, as per the applicant's request, attached evidence, Lawrence Berkeley National Laboratory Team Achieves 10.6 Gigabits/Second Data Throughput in 10-Gigabit Ethernet Test, 07/03/2002, has been provided for the well-known limitations.

57. Regarding the applicant's addition to the limitations, "both TCP network packets and iSCSI instructions embedded in TCP network packets" to the previously rejected claimed subject

matter, the rejections are made under 35 U.S.C. 103(a) rather 35 U.S.C. 102(e) rejections considering the additional limitations.

Conclusion

In order to expedite the prosecution of this case, multiple references are used for the rejections to demonstrate that several references disclose the claimed subject matter of the claims.

Examiner has cited particular columns and line numbers and/or paragraphs and/or sections and/or page numbers in the reference(s) as applied to the claims above for the convenience of the applicant. Although the specified citations are representative of the teachings of the art and are applied to the specific limitations within the individual claim, other passages and figures may apply as well. It is respectfully requested from the applicant in preparing responses, to fully consider the references in entirety, as potentially teaching, all or part of the claimed invention, as well as the context of the passage, as taught by the prior art or disclosed by the Examiner.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Haresh Patel whose telephone number is (571) 272-3973. The examiner can normally be reached on Monday, Tuesday, Thursday and Friday from 10:00 am to 8:00 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nathan Flynn can be reached at (571) 272-1915. The fax phone number for the organization where this application or proceeding is assigned is (571) 273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

/Haresh N. Patel/

Primary Examiner, Art Unit 2454

10/12/08